AMENDMENTS TO THE CLAIMS

Please amend the claims as shown in the following list of all claims presented in this application.

THE INVENTION CLAIMED IS:

1-23. Cancelled.

24. (Currently amended) A semiconductor memory device comprising:

at least one first wordline comprising P-type silicon or polysilicon and a first nonconductive silicon oxide layer;

at least one second wordline comprising N-type silicon or polysilicon and a second nonconductive silicon oxide layer; provided that the second wordline comprises N-type silicon when the first wordline does not comprise P-type silicon; and

wherein the first nonconductive silicon oxide layer is thicker than the second nonconductive silicon oxide layer.

25. (Previously presented) The semiconductor memory device of Claim 24, wherein the first and second nonconductive siliconoxide layers are formed using tetraethylorthosilicate/ozone deposition in a one step process.

26. (Previously presented) The semiconductor memory device of Claim 24, wherein at least one of the first wordline or the second wordline form part of a DRAM array.

27. (Previously presented) The semiconductor memory device of Claim 26 wherein the DRAM array is part of a system-on-chip.

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28. (Previously presented) The semiconductor memory device of Claim 24, wherein at least one of the first wordline or the second wordline form part of an SRAM array.

29. (Previously presented) The semiconductor memory device of Claim 28 wherein the SRAM array is part of a system-on-chip.

30. (Previously presented) A multi-gate semiconductor device comprising:

at least one first P-type gate surrounded by a first nonconductive silicon oxide layer; and

at least one second N-type silicon gate surrounded by a second nonconductive silicon oxide layer;

wherein the first nonconductive layer is thicker than the second nonconductive layer.

31. (Original) The multi-gate semiconductor device of Claim 30, wherein the device is part of a logic circuit.

32-35. Cancelled.

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